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**AMENDMENTS TO THE CLAIMS**

The following listing of claims replaces all prior versions and listings of claims:

**Listing of Claims:**

- 1-5. (Cancelled)
6. (Currently Amended) A [[An]] boundary scan test circuit comprising:  
first and second multiplexers for receiving a shift/capture control signal;  
first and second capture registers coupled to the first and second  
multiplexers, respectively;  
first and second update registers coupled to the first and second capture  
registers, respectively;  
third and fourth multiplexers coupled to the first and second update registers,  
respectively, for receiving a mode control signal;  
a buffer section coupled to the third and fourth multiplexers and to a pad; and  
a first four-input multiplexer receiving the mode control signal and having at  
least one input coupled to the first multiplexer and at least one input coupled to the  
third multiplexer.
7. (Original) The boundary scan test circuit of claim 6 further comprising  
means for enabling EXTEST and INTEST instructions to operate independently.
8. (Original) The boundary scan test circuit of claim 6 further comprising  
means for enabling EXTEST and INTEST instructions to operate simultaneously.
9. (Original) The boundary scan test circuit of claim 6 further comprising  
means for testing a bi-directional pad.
10. (Original) The boundary scan test circuit of claim 6 further comprising  
a second four-input multiplexer having at least one input coupled to an input of the  
first four-input multiplexer.

11. (Original) The boundary scan test circuit of claim 6 further comprising a second four-input multiplexer having at least one input coupled to an output of the first four-input multiplexer.

12. (Currently Amended) The boundary scan test circuit of claim 6 wherein an output of the second four-input ~~[[fourth]]~~ multiplexer provides a control signal for the first four-input multiplexer.

13. (New) A boundary scan test circuit comprising:  
a first multiplexer circuit for receiving a core logic input signal and a shift/capture control signal;  
a capture register circuit coupled to the first multiplexer circuit;  
an update register circuit coupled to the capture register circuit;  
a second multiplexer circuit coupled to the update register circuit for receiving a mode control signal; and  
a buffer coupled to the second multiplexer circuit and to a pad.

14. (New) The boundary scan test circuit of claim 13 further comprising circuitry for enabling EXTEST and INTEST instructions to operate independently.

15. (New) The boundary scan test circuit of claim 13 further comprising circuitry for enabling EXTEST and INTEST instructions to operate simultaneously.

16. (New) The boundary scan test circuit of claim 13 further comprising circuitry for testing a bi-directional pad.

17. (New) The boundary scan test circuit of claim 13 wherein the first multiplexer circuit comprises a four-input multiplexer.

18. (New) The boundary scan test circuit of claim 13 wherein the second multiplexer circuit comprises a four-input multiplexer.

19. (New) The boundary scan test circuit of claim 13 wherein an output of the fourth multiplexer in the second multiplexer circuit provides a control signal for an input of the four-input multiplexer.

20. (New) The boundary scan test circuit of claim 13 further comprising a logic circuit coupled between the first and second multiplexer circuits.

21. (New) The boundary scan test circuit of claim 13 wherein the capture register circuit provides a scan output signal.

22. (New) The boundary scan test circuit of claim 13 wherein the update register circuit receives an update input signal.